IN THE CLAIMS:

Please amend the claims as follows.

5. (Currently Amended) A method of erasing a non-volatile memory cell with a nitride tunneling layer, the non-volatile memory ~~having a substrate, a nitride tunneling layer on the substrate, a charge-trapping layer on the nitride tunneling layer, a dielectric layer on the charge-rapping layer, a gate conductive layer on the dielectric layer, and a source region and a drain region in the substrate beside the gate conductive layer, and the method~~ comprising ~~the steps of~~:

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a substrate;

a nitride tunneling layer disposed on the substrate;

a charge-trapping layer disposed on the nitride tunneling layer;

a dielectric layer disposed on the charge-rapping layer;

a gate conductive layer disposed on the dielectric layer; and

a source region and a drain region disposed in the substrate beside the gate conductive layer;

the method comprising the steps of:

applying a first positive bias to the drain region, applying a second positive bias to the gate conductive layer, and grounding the source region and the substrate to generate hot ~~electron holes~~electron/holes in a channel region, wherein the hot ~~electron holes~~electron/holes are injected into the charge-trapping layer through the nitride tunneling layer.

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6. (Original) The method of claim 5, wherein the first positive bias ranges from about 2V to about 5V.

7. (Original) The method of claim 5, wherein the second positive bias ranges from about 2.5V to about 5V.

8. (Original) The method of claim 5, wherein the first positive bias and the second positive bias are both lower than those adopted for erasing a substrate-oxide-nitride-oxide-silicon (SONOS) memory having a same size as the non-volatile memory with the nitride tunneling layer.

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